Buffer Link Design in a Network on Chip

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Outline

- Motivation
- NoC vs. Bus
- Buffer Link Design
- Results
- Conclusion
- Future Work

- **VAX**: 25%/yr 1978 to 1986
- **RISC+x86**: 52%/yr 1986 to 2002
- **RISC+x86**: ??%/yr 2002 to present
Motivation

Why Chip Multiprocessors?
• Traditional High Performance are less practical
• Power dissipation is a key constraint
• Global wires scale poorly in advanced technologies

<table>
<thead>
<tr>
<th>Manufacturer/Year</th>
<th>AMD/'05</th>
<th>Intel/'06</th>
<th>IBM/'04</th>
<th>Sun/'05</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processors/chip</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Threads/processor</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Threads/chip</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>32</td>
</tr>
</tbody>
</table>
Interconnection for Chip Multiprocessors

- Networks on Chip (NoC) provides a solution for communication-centric chip multiprocessors
- More processing and storage elements integrated
  (Intel 80-core Teraflop, Tilera 64-core, TRIPS, and RAW)
NoC vs. Bus

NoC

Bus
NoC vs. Bus

Bus Advantages:

- Low Complexity
- Low cost
- Well known and commonly used in current architectures
NoC vs. Bus

Bus Disadvantages:

- Do not adapt to changes easily
- New hardware changes means major changes in bus implementation
- Creates communication bottleneck
- Does not scale efficiently
NoC vs. Bus

NoC Advantages:

- Easily Scalable
- Modularity
- Improved Performance
- Minimize the use of global wires
NoC vs. Bus

NoC Disadvantages:

- More complex than bus architectures
- Power and area constraints
Buffer Link Design in NoC

- Design a NoC architecture for low area and low power consumption
Research Work

Problem

- Input buffers account for significant power budget
- Network performance is characterized by input buffers.
Research Work

Approach

- Removing input buffers of routers
- Dual-Function Adaptive Links
Research Work

Simulation

- NoC simulator
- Compare the performance of the original scheme vs. Buffer Link Design
Results

Latency Comparison
Average Difference, High Load 3%
Results

Latency Comparison
Performance degradation: 4% Average high load
Results

Power Comparison
11.27% saved power
Results

Latency Comparison
Performance Degradation: 2%

Modified8buff8links
Original10buff
Results

Power Comparison
18.38% saved power

Power S-Buffer (W)
0.0064
0.0069
0.0074
0.0079
0.0084
0.0089
0.0094
0.0099

Original10buff
8links8buff
Conclusion

- Power and energy saving is really important in chip multiprocessors
- Trade off between power and performance
- With improvement in the buffered link we can save power
- We can save up to 18.38% of power by decrementing the number of input buffers in the router
- Only 4% of throughput loss
Future Work

- Improve further the Dual-Function Adaptive Scheme
- Collect more data to compare the network latency
Questions?